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<u>L5</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L5</u>
<u>L4</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L4</u>
DB=PGPB; PLUR=YES; OP=OR				
<u>L3</u>	<u>L3</u>	L1 and (end near10 transfer)	1	<u>L3</u>
<u>L2</u>	<u>L2</u>	L1 and (address near10 end near10 transfer)	0	<u>L2</u>
<u>L1</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	89	<u>L1</u>

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<u>L7</u>		710/100,300,8,72,305;712/11,14,18;716/16,17;326/38,39,41;439/68.cccls.	11140	<u>L7</u>
<u>L6</u>		l5 and (end near10 transfer)	3	<u>L6</u>
<u>L5</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L5</u>
<u>L4</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L4</u>
		<i>DB=PGPB; PLUR=YES; OP=OR</i>		
<u>L3</u>		l1 and (end near10 transfer)	1	<u>L3</u>
<u>L2</u>		l1 and (address near10 end near10 transfer)	0	<u>L2</u>
<u>L1</u>		processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	89	<u>L1</u>

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L4 and L7	3

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<u>L8</u>	l1 and L7	0	<u>L8</u>
<u>L7</u>	710/100,300,8,72,305;712/11,14,18;716/16,17;326/38,39,41;439/68.ccls.	11140	<u>L7</u>
<u>L6</u>	l5 and (end near10 transfer)	3	<u>L6</u>
<u>L5</u>	processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L5</u>
<u>L4</u>	processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	125	<u>L4</u>
	DB=PGPB; PLUR=YES; OP=OR		
<u>L3</u>	l1 and (end near10 transfer)	1	<u>L3</u>
<u>L2</u>	l1 and (address near10 end near10 transfer)	0	<u>L2</u>
<u>L1</u>	processor near10 cell near10 (configurable or programmable) near10 (function or interconnection or connection)	89	<u>L1</u>


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IEEE JNL IEEE Journal or Magazine

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 1. **Data-driven array processor for video signal processing**

Schmidt, U.; Caesar, K.; Himmel, T.;
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IEEE CNF IEEE Conference Proceeding

 2. **Software detection mechanisms providing full coverage against single bi**

Nicolescu, B.; Savaria, Y.; Velazco, R.;
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 3. **Optimizing Compiler for the CELL Processor**

Eichenberger, A.E.; O'Brien, K.; Peng Wu; Tong Chen; Oden, P.H.; Prener, D.,
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IEEE STD IEEE Standard

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- 6. A 0.8- μ m CMOS two-dimensional programmable mixed-signal focal-plane with on-chip binary imaging and instructions storage**
Dominguez-Castro, R.; Espejo, S.; Rodriguez-Vazquez, A.; Carmona, R.A.; Fo Zarandy, A.; Szolgay, P.; Sziranyi, T.; Roska, T.;
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IEEE STD IEEE Standard

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